Using Average RF Gate and Drain Currents to Determine Gain Compression Mechanisms for Narrow-recessed and Wide-recessed MESFETs

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ABSTRACT: Knee voltage, pinch-off voltage, breakdown voltage and maximum rf drain current clip output I-V waveform of a MESFET and cause gain compression and power saturation. Thus, average rf gate and drain currents can be used to determine gain compression mechanisms for MESFETs. There is a distinct signature in average rf gate and drain currents for each gain compression mechanism. Narrow recess and wide recess MESFET exhibits different average rf gate and drain current behavior when a device is biased toward maximum drain current. The average rf drain current decreases for a wide-recessed MESFET when the device is biased toward maximum drain current and tuned for maximum output power.

INTRODUCTION: A device depending on its bias point suffers from different gain compression mechanism when tuned for maximum output power. Gain compression can be caused by knee voltage, pinch-off voltage, breakdown voltage and maximum rf drain current. A recess structure (gate contour) has great influence on breakdown voltage and the maximum rf drain current. A wide recess structure can increase gate-to-drain breakdown voltage at the cost of lower maximum rf drain current (1). In this paper, gain compression mechanisms for GaAs MESFETs are determined by observing the average rf gate and drain currents. Each clipping mechanism has its distinct signature in average rf gate and drain currents.

DEVICE STRUCTURE AND DC CHARACTERISTICS: Three types of GaAs MESFETs are used in this study. A narrow-recessed MESFET device with doping density of $2.9x10^{17}/cm^3$ and 1 μm gate length is used to study gain compression mechanisms at different bias points. The fabricated device has 1.5 V knee voltage, 200 mA/mm Idss, -2V pinch-off voltage and 13 V gate-to-drain breakdown voltage. Two different recess length MESFET devices with doping density of $2x10^{17}/cm^3$ and 0.7 μm gate length are used to study the effect of gate contour on average rf drain and gate currents. The two devices have the same device and process parameters except different recess length. The corresponding narrow-recessed device has 1.5 V knee voltage, 250 mA/mm Idss, -2V pinch-off voltage and 16 V gate-to-drain breakdown voltage while the corresponding wide-recessed

device has 1.5 V knee voltage, 250mA/mm Idss, -2V pinch-off voltage and 21 V gate-to-drain breakdown voltage.

EXPERIMENTAL RESULTS AND DISCUSSIONS: A commercial ATN load pull system is used here to acquire experimental data. The measured coplanar devices have gate width 6X50 μm for doping density of $2.9x10^{17}/cm^3$ and gate width 10X150 μm for doping density of $2x10^{17}/cm^3$. A CW signal ranging from –15dBm to +10dBm at a fixed frequency of 1.8 GHz is applied to the device in the load pull measurement. The input tuner impedance is set to maximize small signal gain while the output tuner impedance is set to maximize output power at a certain input power. A 10 dBm input power which guarantees the saturation of output power is thus selected to find the optimum output tuner impedance. Large signal performances as a function of input power are then measured at various bias points. The average rf gate and drain currents near P1dB are used to identify the corresponding gain compression mechanism at a given bias point.

The purpose of this paper is to identify the associate signature in rf average gate and drain currents for each gain compression mechanism. Four bias points near only one gain compression region were selected for doping density of $2.9x10^{17}/cm^3$. Figure 1 illustrates power performance, the average rf gate and drain current as a function of input power when Vds=3.5V Vgs=-0.75V (near knee voltage). The average rf gate current is zero and average drain current remains unchanged when gain compression (near P1dB) occurs. In other words, gate is not strongly forward-biased when knee voltage clips output waveform. The power performance and average rf currents when biased at Vds=4.7V Vgs=-1.25V (near pinch-off voltage) are illustrated in figure 2. The operation changes from class A to class AB as input signal becomes larger (2). Thus, the average drain current increases at P1dB. However, gate current is zero because gate is still in reverse bias when gain compression occurs. Breakdown voltage can also cause gain compression and is illustrated in figure 3 for the case of Vds=10V Vgs=-0.75V (near breakdown voltage). The average rf gate current becomes negative and the average rf drain current increases near P1dB. The increase in drain current comes from the generation of positive drain current by avalanche at large drain voltage swing. Also, there exists negative gate current flowing into the gate when the large drain voltage swing reaches breakdown voltage. Figure 4 illustrates power performance and the average rf current when Vds=4.7V Vgs=0V (near maximum drain current). The average rf gate current is zero and average drain current remains unchanged when gain compression (near P1dB) occurs. In other words, the corresponding gain compression mechanism is still knee voltage because the device is tuned for maximum output power and knee voltage limitation gives maximum voltage swing.

Maximum rf drain current gain compression mechanism can be observed in a wide-recessed structure. Narrow-recessed devices and wide-recessed devices with doping density of $2x10^{17}/cm^3$ are biased at

Vds=4.7V Vgs=0V (near maximum drain current) to observe the maximum rf drain current gain compression mechanism. Figure 5 illustrates power performance and average rf current for the case of narrow-recessed device while figure 6 illustrates power performance and average rf current for the case of wide-recessed device. The average rf drain current decreases for the wide-recessed device while the average drain current remains the same for the narrow recessed-device when P1dB occurs. The average rf gate current of the narrow-recessed device is closer to the onset of positive gate current when gain compression occurs. This effect can be explained by the fact that surface depletion caused by the Fermi level pinning blocks current conduction for the case of a wide-recessed structure and thus reduces maximum rf drain current when gate is at its forward rf swing. Thus, the average rf drain current becomes lower as input power becomes higher when biased at Idss for the case of wide recessed device.

CONCLUSION: In summary, all the gain compression mechanisms and their associate signatures have been discussed. Average rf gate and drain currents can be used distinguish different gain compression mechanisms such as knee voltage, pinch-off voltage, breakdown voltage and the maximum rf drain current. Gate contour plays important role in gain compression mechanism. Unintentional excessive undercut in gate recess process can change device power performance dramatically. Thus, the method developed here can help identifying gate contour process variations. Certainly, the method can be directly applied to HEMT devices. An optimum bias point (equally away from these mechanisms) can thus be found through identifying gain compression signatures for the neighboring bias points. The optimum bias point is maximum output power operation in class A mode. With the understanding of gain compression and power saturation mechanism, better large signal performance can be achieved in a device.

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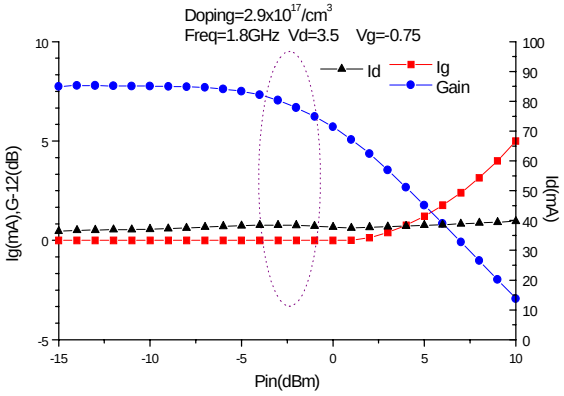

Fig. 1 Gain, Ig and Id vs. Pin when biased near knee voltage.

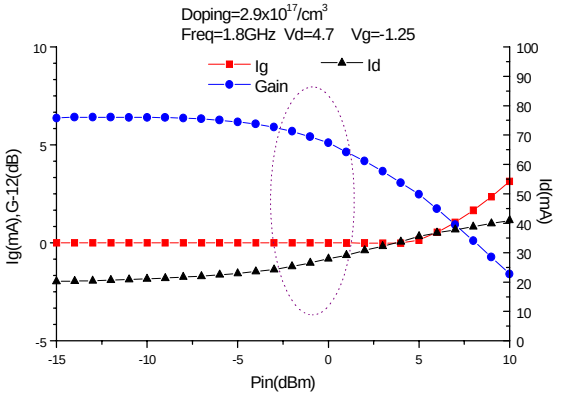

Fig. 2 Gain, Ig and Id vs. Pin when biased near pinch-off voltage

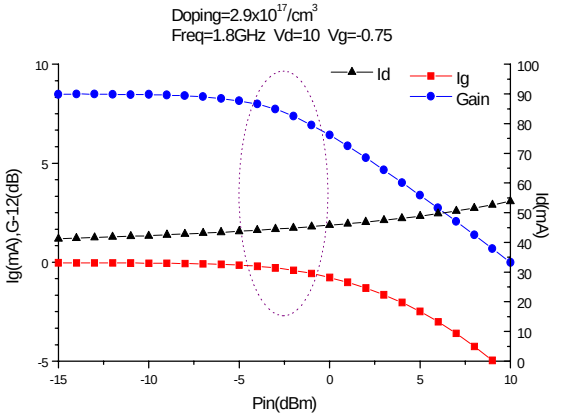

Fig. 3 Gain, Ig and Id vs. Pin when biased near breakdown voltage.

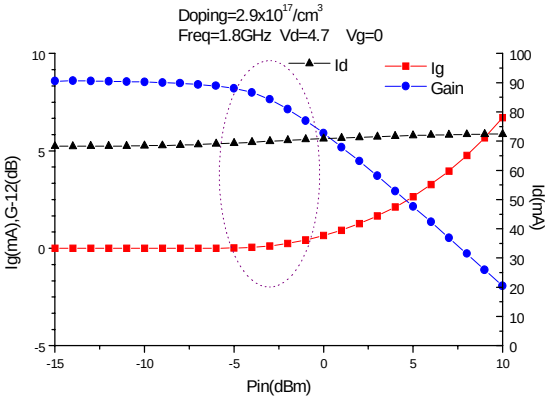

Fig. 4 Gain, Ig and Id vs. Pin when biased near maximum drain current.

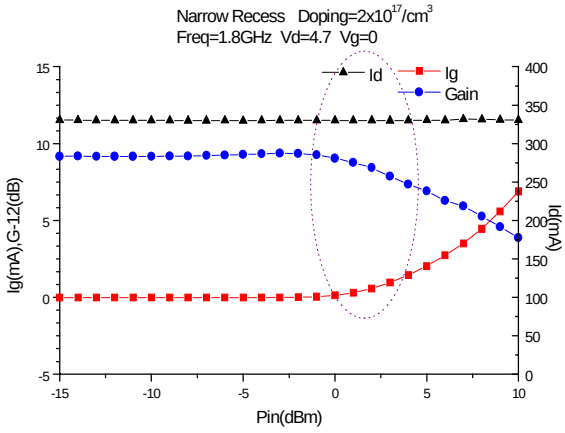

Fig. 5 Gain, Ig and Id vs. Pin when biased near maximum drain current for narrow recessed device.

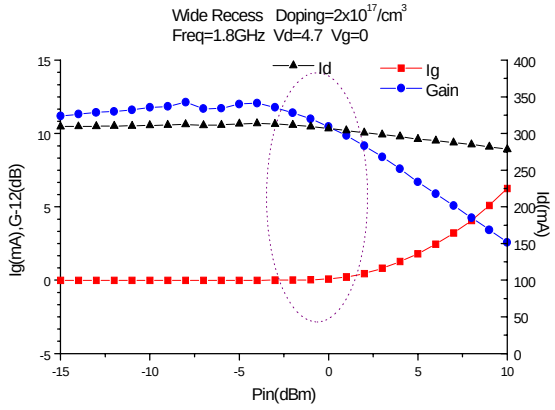

Fig. 6 Gain, Ig and Id vs. Pin when biased near maximum drain current for wide recessed device.